REMARKS

The Office Action mailed August 31, 2004, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Rejection(s) Under 35 U.S.C. § 102 Rejection

Claims 1 – 22 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Lin. Claims 1, 5, 6, 10, 11, 13, 14, 17, 21 and 22 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Irwin. Claims 23 – 32 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Saitoh.

Claim 1 has been amended to more clearly recite the interleaved relationship of the adder and substractor sections of the claimed pipelined averaging filter. Specifically, Claim 1 now states that:

> the at least one subtractor section and the at least one adder section are interleaved with one another such that each adder logic unit of the at least one adder section is coupled to the corresponding adder logic unit of the at least one subtractor section to thereby receive therefrom as a direct input the output of said corresponding adder logic unit of the at least one subtractor section

This feature, supported for example in the second complete paragraph of page 8 of the specification, is not disclosed by either Lin or Irwin. It will be appreciated that, according to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(b) only if each and every claim element is

found, either expressly or inherently described, in a single prior art reference.[1] The aforementioned reasons clearly indicate the contrary, and withdrawal of the 35 U.S.C. § 102(b) rejections based on Lin or Irwin is respectfully urged.

Claim 7 has been amended to recite the following:

> wherein the at least one adder section includes a one delay feedback for each of the plurality of adder logic units and comprises a plurality of bit segments that are different from one another.

In the FIG. 5 arrangement of Lin to which the Office Action makes reference, all the integrators (and differentiators) are identical, as detailed in FIGS. 3a and 3b. By comparison, the filter of Applicant's Claim 7 uses bit segments "that are different from one another," as shown in FIG. 2 and explained in the corresponding discussion at the end of the first complete paragraph of page 9 of the specification. Lin therefore fails to disclose every element of Claim 7, and the rejection of Claim 7 based on Lin is improper and should be withdrawn.

Claim 10 includes states:

> wherein the averaging filter includes a delay enable signal output for each of the plurality of adder logic units of the at least one adder section.

[1] Manual of Patent Examining Procedure (MPEP) § 2131. See also *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Neither Lin nor Irwin disclose this feature. In Lin, FIGS. 3a and 3b disclose applying a on clock delay period (Z-1) to the summer/combiner circuits; however, there is no "delay enable signal *output*" (emphasis added) in the manner of the claimed of the claimed invention. The inventive delay enable signal output is illustrated in Applicant's FIG. 2, and is designated 204 – 209. This output finds no counterpart in either Lin or Irwin.

Claim 12 has been amended to recite that the plurality of adder logic units are "grouped into bit segments that are different from one another." This feature is not disclosed in Lin. Rather, as discussed above, all of the integrators and differentiators of Lin, detailed in FIGS. 3a and 3b, are identical. There are no bit segments are different from one another. Therefore Lin fails to teach all of the limitations of Claim 12 as required for a proper 35 U.S.C. 102(b) rejection.

Claim 13 has been amended in a similar manner to Claim 12, and the same reasoning applies thereto. Claim 13 further recites "a delay enable signal output for each of the plurality of adder logic units." This feature is not disclosed in Lin. Accordingly, withdrawal of the rejection of Claim 13 based on Lin is respectfully urged.

Claim 17 has been amended to recite:

> wherein the at least first processor section and the at least second processor section are interleaved with one another such that each adder logic unit of the at least first processor section is coupled to the corresponding adder logic unit of the at least second processor section to thereby receive therefrom as a direct input the output of said corresponding adder logic unit of the at least second processor section.

As discussed above, this interleaving relationship is not disclosed in Lin or Irwin. Accordingly, Claim 17 is patentably distinct over these references, and the rejection based thereon should be withdrawn.

Claim 23 recites "generating a delay enable signal for each of the plurality of bit segments" and "applying the delay enable signal to each of the processed plurality of bit segments to assemble the output of the pipelined processing." This feature, and its counterpart in Claim 28, is not disclosed in Saitoh. Processing Mask Register 7 of FIG. 1 of Saitoh provides a signal to selectors 6, causing each output selector 6 to perform selection "according to the logic 1 or 0 (1/0 in the figure) from the processing mask register 7." Thus it will be appreciated that no delay is involved, as called for in Applicant's Claims 23 and 28. Saitoh thus fails to teach every limitation of these claims, and the withdrawal of the 35 U.S.C. 102(e) rejection based thereon is respectfully requested.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fee, including those necessary to obtain extensions of time to render timely the filing of the instant Reply, or credit any overpayment not otherwise paid or credited, to our deposit account No. 50-1698.

Respectfully submitted,
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